# Priority Latching Network

## FEATURES

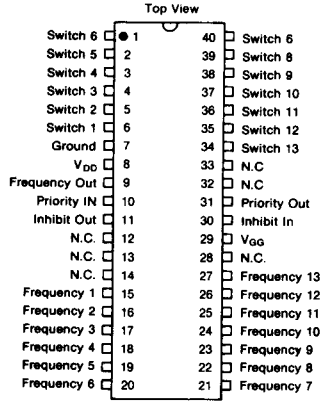
- Low Power Consumption
- Two or more units may be connected in tandem

## DESCRIPTION

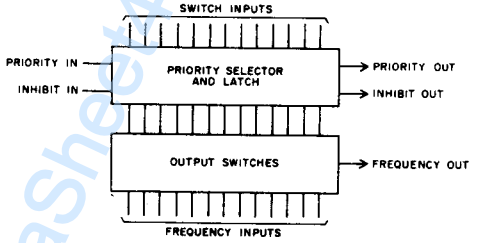
The AY-1-1313 Priority Latching Network is a LSI subsystem designed for use in electronic organ keyboard and pedal latching circuits. When any combination of one or more "switch" inputs is connected to logic "1" the output switch corresponding to the highest priority, or lowest number, input will close, connecting the selected frequency to the output frequency bus. The output switch will remain closed even if the input switch is released, and will remain closed until a new input switch closure occurs.

## PIN CONFIGURATION

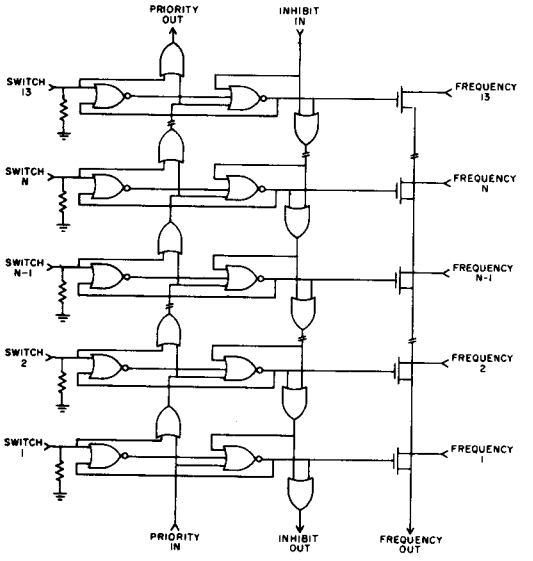
40 LEAD DUAL IN LINE




## BLOCK DIAGRAM




## LOGIC DIAGRAM

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## ELECTRICAL CHARACTERISTICS

### Maximum Ratings*

All Pin Voltages with respect to $V_{SS}$ ..... -30V to +0.3V
Storage Temperature ..... -55°C to +150°C
Operating Temperature ($T_A$) ..... -20°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

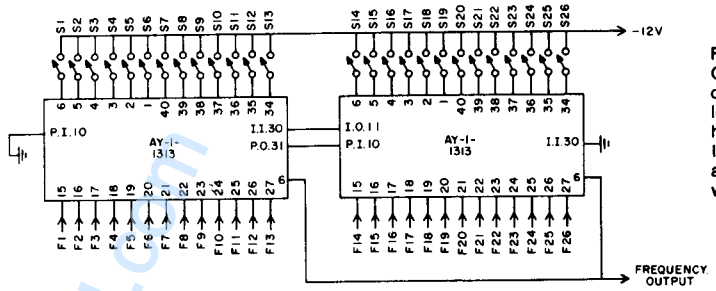
### Standard Conditions (unless otherwise noted)

$V_{DD} = -12 \pm 1V$
$V_{GG} = -27 \pm 1.5V$
$V_{SS} = GND$

| Characteristic | Min | Typ** | Max | Units | Conditions |
|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | |
| Switch Inputs Impedance | 15 | — | 80 | kΩ | Measured to Ground |
| Priority and Inhibit Inputs Impedance | 1 | — | — | MΩ | Measured to Ground |
| Input Logic "0" | — | — | −2 | V | |
| Input Logic "1" | −9 | — | — | V | |
| Output Logic "0" | — | — | −2 | V | $R_L$ = 47K to $V_{DD}$ |
| Output Logic "1" | −9 | — | — | V | $R_L$ = 47K to $V_{DD}$ |
| **Frequency Output Switch** | | | | | |
| Impedance — "ON" | — | — | 20 | kΩ | |
| "OFF" | 5 | — | — | MΩ | |
| $I_{DD}$ Supply Current | — | — | 8 | mA | |
| $I_{GG}$ Supply Current | — | — | 1 | mA | |

**Typical values are at +25°C and nominal voltages.

### TYPICAL APPLICATION




For multiple unit operation, the Priority Output of the higher priority unit is connected to the Priority Input of the lower, and the Inhibit Input of the higher priority unit is connected to the Inhibit Output of the lower. The Priority and Inhibit Inputs must be grounded when not in use.

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